REMARKS

This Amendment responds to the Office Action dated December 10, 2004 in which the Examiner rejected claims 1-4 under 35 U.S.C. §112, second paragraph, rejected claim 1 under 35 U.S.C. §102(b) and rejected claims 2-4 under 35 U.S.C. §103.

As indicated above, claims 1 and 4 have been amended in order to more particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Applicant respectfully submits that the amendment does not narrow the literal scope of the claim. In particular, support can be found on page 13, lines 24,27, page 15, lines 1-15, page 18, lines 7-8, etc. Therefore, applicant respectfully requests the Examiner withdraws the rejection to claims 1-4 under 35 U.S.C. §112, second paragraph.

Claim 1 claims a semiconductor device comprising an electrode formed of a flat plate portion at a bottom thereof and a cylindrical portion which extends up continuously from the flat plate portion and whose one side is open. A surface roughness due to grains on an outer surface of the electrode is larger than a surface roughness of an inner surface of the electrode.

Through the structure of the claimed invention having an electrode with an outer surface having a larger surface roughness than an inner surface thereof, as claimed in claim 1, the claimed invention provides a semiconductor device in which not only the surface on which growth nuclei is placed is enlarged but also the opposite surface so that the occurrence of a short circuit between capacitor electrodes is prevented. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claims 4 claims a semiconductor device comprising an electrode formed of a cylindrical portion and a conductive film buried in the inner side of the cylindrical portion. A surface roughness due to grains on an outer surface of the electrode is larger than a surface roughness on an inner surface of the electrode.

Through the structure of the claimed invention having an electrode with a surface roughness of an outer surface larger than that of the inner surface as claimed in claim 4, the claimed invention provides a semiconductor device in which growth nuclei enlarges the surface area on the side opposite to where the growth nuclei is placed and thus prevents short circuiting of the capacitor electrode. The prior art does not show, teach or suggest the invention as claimed in claim 4.

Claim 1 was rejected under 35 U.S.C. §102(b) as being anticipated by *Figura et al* (U.S. Patent No. 5,763,286).

Figura et al appears to disclose a low-cost process for manufacturing a dynamic random access memory capacitor having an annularly-grooved, cup-shaped storage-node plate which stores charge on inner and outer surfaces. (col. 1, lines 12-15) Referring now to FIG. 3, following a masking step, mold openings 31 have been etched in the mold layer 23 using an anisotropic plasma etch. Each mold opening penetrates the mold layer 23 and the etch stop layer 18 so as to expose the top of each storage-node contact plug 17A. Referring now to FIG. 4, a wet etch step is employed which selectively etches the second material layers 22 at a faster rate than the first material layers 21. The selective etching creates a pattern of annular grooves 41 within each mold opening 31. Referring now to FIG. 5, a storage-node plate layer 51 has been blanket deposited over the array depicted in FIG. 4. It will be noted that the storage-node plate layer 51 has covered the upper surface of the mold

layer 23 and the interior of the mold openings 31. Because CVD typically forms deposited layers which conform well to irregularly-shaped surfaces and which display excellent step coverage, the grooves within mold openings 31 are conformally coated with polysilicon layer 51. It will be noted that the annular grooves 41 (see FIG. 4) within mold openings 31 are narrow in relation to the thickness of storage-node plate layer 51. Thus, the exposed surface of storage-node plate layer 51 is smooth. Referring now to FIG. 6, an optional rough capacitance-enhancing surface has been formed on the exposed surface of polysilicon layer 51 through the formation of hemispherical grain polysilicon protuberances 61 thereon. Referring now to FIG. 7, that portion of the polycrystalline silicon layer 51 that is on the upper surface 71 of the mold layer 23 has been removed. Referring now to FIG. 8, the remaining portion of mold layer 23 has been removed. In the case where both first and second material layers (21 & 21) are both various forms of TEOS oxide, a single wet silicon dioxide etch is employed. A plasma etch, although generally less selective than certain wet etches, may also be employed to remove the mold layer 23. It will be noted that the wall portion 74 of each storage-node plate 72 has an outer perimetric surface 81 on wall portion 74 (see FIG. 7) and an inner perimetric surface 82 on wall portion 74 (see FIG. 7). The outer surface 81 has a plurality of perimetric grooves 83 which are stacked one on top of another. Charge will be stored on the upper surface 84 of each floor portion 73 (see FIG. 7), on the outer surface 81, and on the inner surface 82. The grooves 83 enhance the charge storing capacity of the outer surface 81, while the hemispherical-grain polysilicon protuberances 61 on the inner surface 82 enhance the charge storing capacity of the inner surface 82. (col. 5, line 1 through col. 6, line 18) Referring now to the FIG, 11

photograph, a plurality of storage-node plates are shown in a combination of both cross-sectional views (foreground) and perspective views (background). At this stage of fabrication, there has been no deposition of hemispherical grain polysilicon protuberances, no deposition of a capacitor dielectric layer, nor deposition of a cell plate layer. As can be seen from the dimension scale superimposed on the photograph, these structures are of a size that is appropriate for use in a 256-megabit dynamic random access memory. (col. 6, lines 42-51)

Thus, *Figura et al.* merely discloses in Fig. 11 grooves formed parallel to the substrate and is called fin-type. Nothing in *Figura et al.* shows, teaches or suggests surface roughness due to grains as claimed in claim 1 (and claim 4).

Also, *Figura et al* merely discloses in FIGS. 5-8 coating mold opening 31 with a polysilicon layer 41 which covers grooves 41 formed within the mold opening 31. Thus, nothing in *Figura et al* shows, teaches or suggests a) a surface roughness due to grains on both outer and inner surfaces of an electrode, b) the outer surface has a larger surface roughness due to grains than the inner surface and c) the surface roughness is based upon grains as claimed in claim 1 (and claim 4). Rather, *Figura et al* merely discloses coating a polysilicon layer 51 into the mold opening 31 in order to cover the grooves 41.

Since nothing in *Figura et al* shows, teaches or suggests surface roughness due to grains on an outer surface of an electrode is larger than surface roughness on an inner surface of the electrode as claimed in claim 1, applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(b).

Claims 2-4 were rejected under 35 U.S.C. §103 as being unpatentable over *Figura et al* and further in view of *Sandhu et al* (U.S. Patent No. 5,754,390).

As discussed above, *Figura et al* merely discloses forming grooves parallel to the substrate and coating a polysilicon layer 51 in order to coat grooves 41 within mold openings 31. Nothing in *Figura et al* shows, teaches or suggests surface roughness due to grains on an outer surface of an electrode is larger than surface roughness of an inner surface of the electrode as claimed in claim 4. Rather, *Figura et al* merely discloses that the grooves 41 within the mold 31 are coated with a polysilicon layer 51 by CVD and that the grooves are formed parallel to the substrate.

Sandhu et al appears to disclose fabrication of capacitor bottom electrodes for high performance dynamic random access memory (DRAM) chips. (col. 1, lines 8-9) In the embodiments described herein, the first electrode layer 22 comprises a polysilicon layer in contact with a transistor active area 25, in a contact via, trench, or container. (col. 3, lines 46-49) The first electrode layer 22 of the preferred embodiments, however, has a roughened surface in the form of hemispherical grained silicon (HSG polysilicon), which may be achieved by any known method. (col. 3, lines 58-61) The strap 20 improves the overall bottom electrode conductivity, such that the polysilicon of the first electrode layer 22 need not be doped as heavily as prior art HSG polysilicon 10 (FIG. 1) would require. (col. 4, lines 7-10)

Thus, *Sandhu et al* merely discloses a conductive strap 20. Nothing in *Sandhu et al* shows, teaches or suggests a surface roughness due to grains on an outer surface of the electrode is larger than the surface roughness on an inner surface of the electrode as claimed in claim 4. Rather, *Sandhu et al* merely discloses a conductive strap 20.

Since neither *Figura et al* nor *Sandhu et al* shows, teaches or suggests a surface roughness due to grains on an outer surface of the electrode is larger than the surface roughness on an inner surface of the electrode as claimed in claim 4, applicant respectfully requests the Examiner withdraws the rejection to claim 4 under 35 U.S.C. §103.

Claims 2-3 depend from claim 1 and recite additional features. Applicant respectfully submits that claims 2-3 would not have been obvious within the meaning of 35 U.S.C. §103 over *Figura et al* and *Sandhu et al* at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 2-3 under 35 U.S.C. §103.

New claims 11-14 have been added and recite additional features. Applicant respectfully submits that these claims are also in condition for allowance.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time.

The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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